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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/597,353	07/06/2007	Yoshito Katano	09792909-6735	9812

26263 7590 02/02/2010

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EXAMINER	
WILSON, YOLANDA L	

ART UNIT	PAPER NUMBER
2113	

MAIL DATE	DELIVERY MODE
02/02/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/597,353	KATANO ET AL.	
	Examiner	Art Unit	
	Yolanda L. Wilson	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 November 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/09/2009*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 1-6,8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lambino et al. (US Publication Number 20020073358A1) in view of Curry et al. (USPN 6032248). As per claims 1 and 8, Lambino et al. discloses a semiconductor device and a data-rewritable nonvolatile memory, said data-rewritable nonvolatile memory having a plurality of data blocks wherein boot program instructions are stored in parallel said boot program instructions, said semiconductor device comprising a central processing unit (CPU) and a read control circuit (RCC), wherein: the RCC is configured to (a) determine whether the first respective data block is faulty or not according to data read out from the first respective block, (b) output the first data to the CPU if the block is determined as not faulty, and (c) read when the first respective data blocks is determined as faulty, second data from the second respective data block and output said second data to the CPU when said second respective data block is determined as not faulty in Figure 3; paragraphs 0020-0021.

Lambino et al. fails to explicitly state comprising a plurality of pages of data, each said page being stored in parallel in at least two data blocks; and the CPU is configured, in part, to specify to the RCC a read position for reading out each page of the boot

program instructions stored in the data-rewritable nonvolatile memory at the starting time, said each page stored in parallel in at least a first respective data block and a second respective data block.

Curry et al. discloses these limitations in column 12, lines 12-21.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have comprising a plurality of pages of data, each said page being stored in parallel in at least two data blocks; and the CPU is configured, in part, to specify to the RCC a read position for reading out each page of the boot program instructions stored in the data-rewritable nonvolatile memory at the starting time, said each page stored in parallel in at least a first respective data block and a second respective data block. A person of ordinary skill in the art would have been motivated to have comprising a plurality of pages of data, each said page being stored in parallel in at least two data blocks; and the CPU is configured, in part, to specify to the RCC a read position for reading out each page of the boot program instructions stored in the data-rewritable nonvolatile memory at the starting time, said each page stored in parallel in at least a first respective data block and a second respective data block because the page information discloses how the data is stored in memory.

3. As per claim 2, Lambino et al. discloses wherein the read control circuit is configured to determine whether the block is faulty or not faulty at least according to an error correction code contained in the data read out from the data-rewritable nonvolatile memory in paragraph 0023.

4. As per claim 3, Lambino et al. discloses wherein the read control circuit corrects the data and supplies it to the CPU when it determines that the data is correctable according to the error correction code but otherwise determines that the block is faulty when it determines that the data is uncorrectable data in paragraph 0023.

5. As per claim 4, Lambino et al. discloses wherein the read control circuit is configured to determine that the block is faulty or not faulty at least according to a block state information contained in the data read out from the data-rewritable nonvolatile memory in paragraphs 0020-23.

6. As per claim 5, Lambino et al. discloses wherein the read control circuit determines that the block is faulty when the block state information does not show a predetermined value in paragraphs 0020-23.

7. As per claim 6, Lambino et al. fails to explicitly state wherein the block state information is stored in a leading page of each of the blocks storing boot program instructions.

Curry et al. discloses these limitations in column 12, lines 12-21.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have wherein the block state information is stored in a leading page of each of the blocks storing boot program instructions. A person of ordinary skill in the art would have been motivated to have wherein the block state information is stored in a leading page of each of the blocks storing boot program instructions because the page information discloses how the data is stored in memory.

8. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lambino et al. in view of Aasheim et al. (USPN 7178061B2). As per claim 7, Lambino et al. and Hashimoto fail to explicitly state wherein the data-rewritable nonvolatile memory is a NAND type flash memory.

Aasheim et al. discloses this limitation in column 9, lines 20-25.

Accordingly, a person of ordinary skill in the art would be motivated to have the data-rewritable nonvolatile memory is a NAND type flash memory. A person of ordinary skill in the art would be motivated to have the data-rewritable nonvolatile memory is a NAND type flash memory because NAND type flash memory is a known type of non-volatile memory used for storing boot programs.

Response to Arguments

9. Applicant's arguments with respect to claims 1-8 have been considered but are moot in view of the new ground(s) of rejection. The newly added limitations to the claims required a new reference to be found. Please see the above rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yolanda L. Wilson whose telephone number is (571) 272-3653. The examiner can normally be reached on M-F (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Yolanda L Wilson/
Primary Examiner, Art Unit 2113